A RADIO ARCHITECTURE COMPLIANT WITH ECMA-392 STANDARD FOR PERSONAL WHITE SPACE DEVICES

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ABSTRACT

Wireless devices which operate in the TV-white spaces, unused regions of the frequency spectrum, have recently gained much attention. These devices find a variety of applications such as in wireless rural broadband access which has attracted interest from developers worldwide. The FCC and other commissions worldwide defined specifications for devices which operate in these frequency bands. These specifications emphasize minimum interference with incumbent signals. This paper presents an architecture for the baseband part of such white space devices, specifically the ADC and DAC architectures, and proposes tentative block level specifications for baseband blocks in both the receive and transmit chains making them suitable for low power full system-on-chip integration in bulk CMOS. Coupled with our own recently derived RF front end specifications, the proposed overall radio transceiver architecture meets the ECMA-392 specification, one of the first standards published worldwide which specifies a medium access control (MAC) layer and a physical layer for personal/portable white space devices.

1. INTRODUCTION

When TV stations transitioned from analog to digital transmission, parts of the TV spectrum were rendered unused. These spectrum holes are referred to as white spaces. Specifically, the white spaces in the TV band are referred to as TV white spaces. The ultra high frequency (UHF) TV frequency band in the United States ranges from 512 MHz to 698 MHz vis-à-vis channel 21 to 51. Each channel in this band has a channel bandwidth of 6MHz. All channels in this band are available to white space devices except channel 37 which is reserved for radio astronomy measurements.

Federal communications commission (FCC) and other commissions worldwide issued regulatory rules for radio use of the TV white space spectrum. The devices operating according to these regulations are called TV Band Devices which are of two classes – fixed and personal. European Computers Manufacturing Association (ECMA) – 392[1] is one of the first standards published that specifies a physical layer personal white space devices operating in the TV band. The ECMA-392 specification is briefly introduced in [2].

We recently derived the specifications for the Radio Frequency (RF) Front end to meet the specifications provided by ECMA-392[2]. In this paper, the specification for the baseband is derived. Different architectures are explored for Analog to Digital converters (ADCs) and Digital to Analog converters (DACs) and the pros and the cons of each architecture is examined. Based on the study of the various architectures and the specifications desired, a baseband architecture is proposed for personal white space devices.

The paper is organized as follows. Section 2 derives the specification desired for the baseband. Section 3 surveys the various architectures of ADCs and DACs and proposes an architecture. Section 4 presents simulation results. Section 5 concludes the paper.

2. BASEBAND SPECIFICATION

As stated in an earlier work of ours, [2] transceiver architecture for personal white space devices consisting of a homodyne receiver and a heterodyne transmitter has been proposed. In addition to the reasons stated in [2] the homodyne receiver also helps exploit better Signal to Noise ratio (SNR) performances of the ADC at lower frequencies thereby making the specification easier to achieve for all blocks concerned. Also, down-converting the radio signal to baseband ensures that the power consumption of the ADC is reduced and subsequently the power consumption of the receiver chain is optimized.

The most critical constraint while deriving the specifications for the baseband is the power efficiency of the design. Although, the target applications of white space devices are not necessarily handheld, the most important application of white space devices is for rural areas. Hence

these devices will have to be able to withstand unreliable power supply and long stretches of not being powered. Hence, it is vital that white space devices are designed to optimize power efficiency as well. As stated in [3] ADCs are one of the most power hungry blocks of the receiver chain.

The specifications of the ADC that affect the system level performance include the resolution of the ADC. The following assumptions are made while deriving system specifications for the ADC. The channel bandwidth of each TV channel varies from 6-8 MHz. Anticipating a provision for being allowed to transmit on contiguous channels, a channel bandwidth of 24MHz (four contiguous channels) is assumed. For this bandwidth a sampling frequency of 80MHz is chosen.

ECMA-392 specification requires a noise figure of 6dB for the entire receiver chain. However, designing for a safety margin, the ADC specifications are designed for a receiver noise figure of 5.6dB. Making the same assumption for the noise floor as before, i.e. -100dBm, the minimum SNR, SNRmin, that the receiver should have as per the ECMA-392 specification is 8dB. Hence, the minimum SNR required from the ADC output can be found to be 2.4dB. A blocking signal of power 70dB higher than the required minimum detectable signal (approximate average power of an NTSC signal) is assumed. The specifications for the ADC are then obtained using the equations defined in [4]. The minimum bit resolution is found to be 11.86bits. However, this resolution has been calculated only taking into account SNR considerations while neglecting ADC non linear effects. A more appropriate and realistic way of deriving the ADC resolution requirements is by considering the spurious free dynamic range (SFDR) of the ADC. SFDR is a critical ADC performance measure especially for wideband receivers [5]. The required SFDR is computed using the equation defined in [4] and is calculated to be 72.4dB which translates to approximately 12 bits of resolution.

The system ADC specifications are found out to be as follows. As stated before, a sampling frequency of 80MHz has been chosen. For this sampling frequency and the assumptions stated above, the required resolution of the ADC is 13 bits. An extra 1 bit of resolution is added as a margin for other noise such as thermal noise, flicker noise etc. that can enter the system and degrade the ADC performance and hence the system performance.

The requirement on the transmitter signal quality by the standard, i.e. the error vector magnitude (EVM) determines the resolution of the DAC. ECMA-392 requires an EVM of -11.7dB as part of its specification. For the specifications of the RF block of the transmitter mentioned in [2] an EVM of -15.6dB is achieved thereby leaving enough margin for the DAC non-linearity and other sources of noise such as supply voltage noise etc. [6] provides a comprehensive analysis of modeling DACs for telecommunications.

As suggested in [6], the impact of mismatch is reduced when the oversampling ratio is increased. Keeping this in mind, a sampling frequency of 80 MHz is selected for the DAC, same as that for the ADC. A first cut approximation for the resolution of the DAC is also inferred from the results stated in [6]. A resolution of 10 bits is selected to provide a Signal to Noise and Distortion Ratio (SNDR) of the order of 60dBc. This ensures that the EVM specification of the standard is still observed leaving enough margin for other sources of noise.

3. ARCHITECTURE

[3][7] do a thorough survey and analysis of existing ADC architectures. A brief overview of ADC architectures follows. ADC architectures can be broadly classified into Successive approximation (SAR), Integrating ADCs, oversampling ADCs and Flash ADCs. Integrating ADCs and SAR implementation usually involves a lot of charge transfer between capacitors which severely limits the bandwidth of the ADC operation. Oversampling ADCs offer a tradeoff between resolution and bandwidth offering high resolution at the expense of reduced bandwidth. Flash ADCs convert the fastest but offer limited resolution with scaling technology. Pipeline ADCs can be seen as a derivative of Flash ADCs where chunks of bits are accounted by Flash ADCs and all the chunks are added together thereby providing high resolution high bandwidth ADCs. Figure 1 illustrates the areas of application as a function of resolution and speed of these architectures.

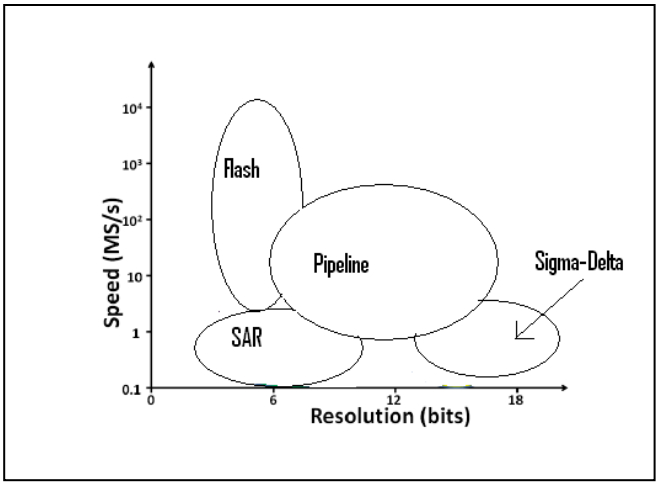

Fig 1. Application specific ADC architectures - overview

For the specifications derived in the previous section, the natural choice of architecture for the ADC is the pipeline ADC. There are multiple reasons for this. The sampling frequency is too high for integrating ADCs. Successive approximation ADCs which invariably use charge transfer between capacitors are not very accurate at high frequencies. Flash ADCs have historically never been used for high resolution for a multitude of reasons – complexity of design for higher resolution, large number of comparators, large chip area and higher power consumption etc. The input bandwidth requirement may require a high sampling frequency for delta sigma ADCs that could exceed 1GHz. Since the receiver chain, from the antenna to the input of the ADC, requires a high gain, in excess of 60dB, it may not be easy to achieve such high gain in a nanometer (sub 65nm) node. Hence, it would be difficult to design a power efficient delta sigma ADC for the derived ADC system specification. Therefore, pipeline ADCs appear to be the best choice for the given specifications. Pipeline ADCs have comparatively higher latency but have a high throughput. Pipeline architecture has the advantages of Flash ADCs while being less complex to design and more power efficient thereby enabling us to use this architecture to design higher resolution high bandwidth ADCs.

Pipeline ADC architecture has been discussed in great detail in [8]. Each stage of a pipeline ADCs can be thought of broadly as consisting of a sample and hold block, an ADC, a DAC block and a gain block. The key factor impacting the number of stages and the number of bits per stage of the pipeline is the power efficiency. ADC and DAC blocks are not dominant factors in the power consumption of the pipeline. As stated in [7] the majority of the power consumed by each pipeline stage is by the operational amplifier (Op-Amp) as part of the sample and hold circuitry. It can be easily verified that for a 13 bit ADC, the least number of comparators are used when a three stage – five bit – four bit – four bit – pipeline ADC is used.

Similarly, for the DAC, the specifications derived in the previous section suggest a current steering architecture for the DAC. The string architecture is slow because of the RC delays. Current steering DACs are popularly used for telecommunication purposes and have been discussed in detail in [6]. Assuming a finite output resistance for the current sources (source resistance) and a non-zero resistance for the switch (load resistance) the DAC specification can be obtained for a source to load resistance ratio of the order of 10^7. Also, a current mismatch of no more than the order of 10^{-3} is required to meet the DAC specifications.

The following section looks exclusively at simulation results of Pipeline ADC modeled using MATLAB.

4. SIMULATION RESULTS

A 13 bit 3 stage Pipeline ADC architecture discussed in the previous section is modeled on MATLAB using Simulink. The behavioral model as an input accepts a sinusoid wave with a frequency that can be set by the user. On simulation, the power spectral density at the output is plotted and the SNR, and thus the bit resolution, of the ADC is verified. As an input signal, various sinusoids varying in frequency from 1MHz to 6MHz have been used. Before looking at the simulation results, the model is briefly explained.

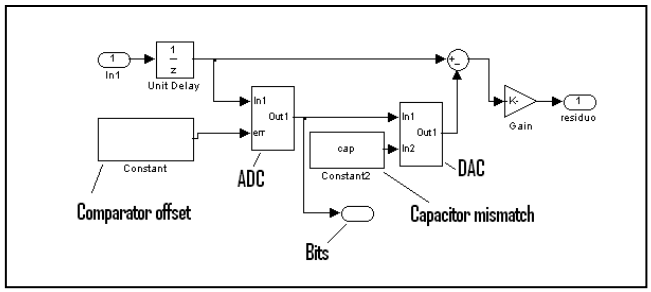

Fig 2: Top level model of a single pipeline stage

Figure 2 illustrates the top level model of a single pipeline stage. The input passes through a sample and hold amplifier, modeled using a delay element. The output of the sample and hold stage is fed to an ADC. The behavioral model of the ADC is illustrated in Figure 3. Physically, this ADC can be built using Flash ADC architecture. The block 'cap' in Fig 2 is used to introduce mismatch errors in capacitors to the model.

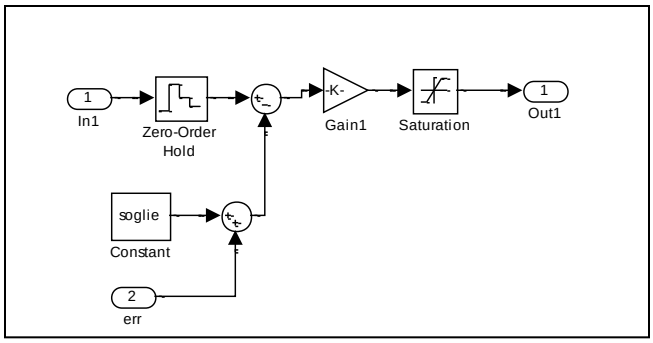

Fig 3: Behavioral model of ADC block of a single pipeline stage

The ADC model is illustrated in Fig 3. A comparator offset error is introduced using the 'err' block. The saturation block helps model the comparator behavior. An upper and lower limit of 1 and -1 respectively is set thereby reflecting the behavior of a comparator. The gain in the gain block is set to an arbitrarily large gain value as is typical in operational amplifiers.

Modeling the DAC is straightforward. The error between the 'held' input signal and the DAC output is then amplified in order to relax the specifications for the blocks in the subsequent stages. In the case of 5 bit pipeline stage, the gain in the gain block is 32 and in the 4 bit pipeline stage the gain is 16 thereby providing the stages with 5 bit and 4 bit resolution respectively.

Fig 4, below, illustrates the complete 13 bit pipeline ADC model. The error signal generated at each stage is used as input to the subsequent stage to obtain the next most significant bits. By adding simple digital correction the performance of the ADC can be further improved.

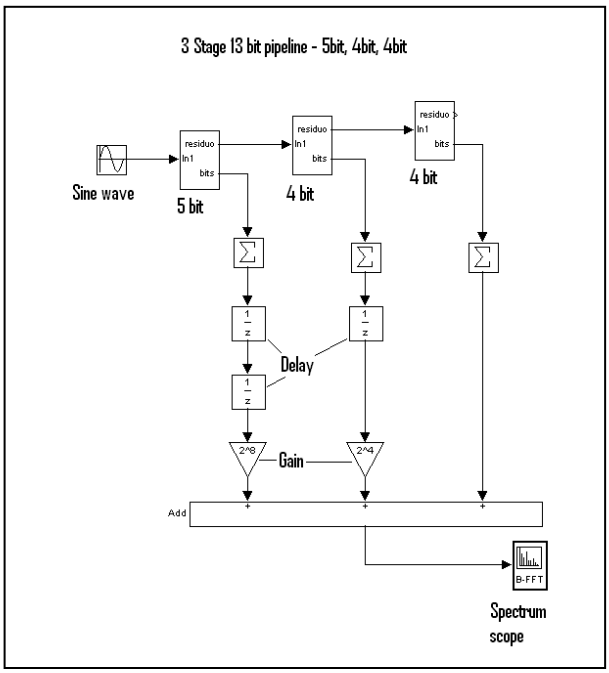

Fig 4: Behavioral model for a 3 stage 13 bit pipeline ADC

Fig 5 illustrates the power spectral density at the output of the pipeline ADC. The signal input is 1.24MHz sinusoid. A capacitor mismatch error of 1% is introduced to the 64 capacitors that are needed for the DACs. (32 capacitors for the 5-bit stage and 16 capacitors each for the two 4-bit stages). A threshold error is introduced for each of the 64 comparators required for the design. Also, a gain error of 5% is introduced for the gain amplifier at the end of each pipeline stage.

From Fig 5 it can be verified that an SNR of the order of 75dB is achieved which translates to a 13-bit resolution. Hence, for the above design margins the baseband meets the required specifications. The model was simulated for other input frequencies as well and the ADC system specifications were verified. It must be noted that the rest of the system specifications are the same as that mentioned in section 3 i.e. a sampling frequency of 80 MHz is used.

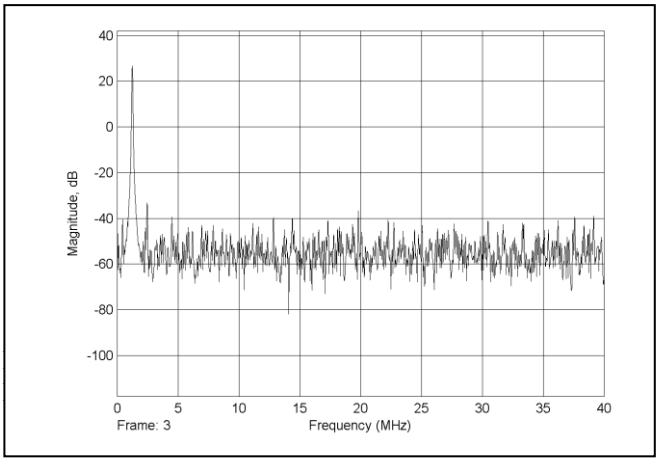

Fig 5: Power Spectral Density at the output of 13-bit Pipeline ADC

5. CONCLUSION

Baseband specifications, given our previously derived RF front end specification, have been derived. Resolution in terms of number of bits and the sampling frequency for the ADC and DAC have been proposed. Given the system specifications for the ADC, a pipelined architecture has been proposed. Given the system specifications for the DAC a current steering architecture has been proposed as it is optimal for the high sampling frequency of the DAC. Design margins for current mismatch and non idealities in terms of current source resistance and switch resistance are provided for the DAC. Design margins for capacitance mismatches, gain error and threshold error have been made and the proposed system level architecture for the ADC has been verified. Future work will focus on nanometer CMOS system-on-chip implementation of the proposed architecture.

6. REFERENCES

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